In the Claims:

No amendments to the claims are presented

1. (Previously presented) A power semiconductor device, comprising:

an output transistor having

main cells and sense cells,

a control input connected to the main and sense cells, and

main and sense cell controlled outputs;

an output terminal connected to one of the main cell controlled outputs for connection to a load;

a feedback circuit for measuring the voltage across the main cell controlled outputs of the output transistor and controlling the voltage on the control input to increase the voltage across the main cell controlled outputs if the magnitude of the voltage across the controlled outputs falls below a predetermined value;

a reference current supply feeding a reference current through the sense cell controlled outputs; and

a comparator arranged to compare the voltages across the main cell outputs and the sense cell outputs and to output a low-current signal when the magnitude of the voltage across the main cell outputs falls below that across the sense cell outputs.

2. (Previously presented) A power semiconductor device according to claim 1 wherein the feedback circuit includes a voltage reference and a comparator connected across the main cell outputs for comparing the voltage across the main cell outputs with the voltage reference, the output of the comparator of the feedback circuit being connected through a diode to the control input, the diode being orientated to pass current to change the control voltage in a direction to increase the on-resistance of the main cells when the voltage across the main cell outputs falls below the predetermined value.

3. (Previously Presented) A power semiconductor transistor according to claim 1 wherein the main and sense cells are FET main and sense cells and the gates of the FETs are connected in common to the control input and the sources and drains of the FETs of

the main and sense cells form the outputs of the FETs.

4. (Previously presented) A power semiconductor device according to claim 3, in the form of a high side device wherein:

the drains of the sense and main cells are connected in common to a battery terminal;

the source of the main cells is connected to the output terminal; and

the source of the sense cells is connected to the reference current supply, the reference current supply being a reference current sink.

5. (Previously presented) A power semiconductor circuit including a semiconductor device according to claim 1 further comprising a load connected to the output terminal.

6. (Previously presented) A method of operating a semiconductor device, the device including an output transistor having main cells and sense cells, a control input connected to the main and sense cells, and main and sense cell controlled outputs, the method comprising:

driving the main and the sense cells in common;

driving a load from one of the main cell controlled outputs feeding a reference current through the sense cell controlled outputs;

measuring the voltage across the main cell controlled outputs and controlling the voltage on the control input to increase the voltage across the main cell controlled outputs if the magnitude of the voltage across the main cell controlled outputs falls below a predetermined value; and

comparing the voltages across the main cell controlled outputs and the sense cell controlled outputs and outputting a low-current signal when the magnitude of the voltage across the main cell controlled outputs falls below that across the sense cell controlled outputs.

7. (Previously Presented) A method according to claim 6 wherein the step of measuring the

voltage across the main cell controlled outputs is performed by:

comparing the voltage across the main cell controlled outputs with a reference voltage using a comparators; and

driving the control input from the output of the comparator through a diode the diode being orientated to pass current to change the control input voltage in a direction to increase the on-resistance of the main cells when the voltage across the main cell outputs falls below the predetermined value.